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A Design of 0.7-V 400-MHz All-Digital Phase-Locked Loop for Implantable Biomedical Devices

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SUMMARY A low-voltage controller-based all-digital phase-locked loop (ADPLL) utilized in the medical implant communication service (MICS) frequency band was designed in this study. In the proposed design, controller-based loop topology is used to control the phase and frequency to ensure the reliable handling of the ADPLL output signal. A digitally-controlled oscillator with a delta-sigma modulator was employed to achieve high frequency resolution. The phase error was reduced by a phase selector with a 64-phase signal from the phase interpolator. Fabricated using a 130-nm CMOS process, the ADPLL has an active area of 0.64 mm^2, consumes 840 μW from a 0.7-V supply voltage, and has a settling time of 80 μs. The phase noise was measured to be −114 dBc/Hz at an offset frequency of 200 kHz.

key words: *all-digital phase-locked loop, controller, digitally-controlled oscillator, phase interpolator, CMOS, MICS*

1. Introduction

Biomedical radio-frequency (RF) transceivers require miniaturized forms with a long battery life and low power consumption. It is usually preferable for implantable medical devices to be fully-integrated on a single chip to realize easier surgery and encapsulation for high biocompatibility. The medical implant communication service (MICS) band in the frequency range of 402 to 405 MHz is widely used for medical RF transceivers because MICS band signals have reasonable propagation characteristics in the human body and are well suited to achieve a good trade-off between size and power [1], [2].

There are many challenges associated with the implementation of the RF front-end in implantable medical devices such as pacemakers, implantable cardioverter defibrillators, and neurostimulators because their application requires extremely low power consumption, minimal external components, and high reliability. The basic system requirements of RF transceivers for medical implantable devices are as follows [2]. To increase battery life, the current of RF transceivers should be limited to below 6 mA during MICS band communication. The use of few external components provides a higher reliability, lower cost, and smaller size. RF modules for pacemakers must be no more than approximately 3 mm × 5 mm × 10 mm. Pacemaker applications currently demand a reasonable data rate of over 20 kbps with higher data rates projected for the future. Their operating range is typically over 2 m because the MICS band is designed to improve upon the very-short-range inductive link.

In particular, the frequency synthesizer is one of the most critical building blocks of the RF front-end. Phase-locked loops (PLLs) are widely used in many communication systems to perform frequency synthesis or clock and data recovery. Analog PLLs based on charge-pumps are still widely used, but all-digital PLLs (ADPLLs) have been attracting more attention because of their significant advantages over their analog counterparts. ADPLLs, which interface to allow peripheral circuitry to be digitally implemented, provide low-voltage operation compatibility under process and temperature variations with a shorter system turnaround-time [3]. Hence, ADPLLs provide several benefits to duty-cycled battery-operated systems, including MICS transceivers, wireless sensor nodes, and wireless telemetry devices. In the design of an ADPLL, realizing a low level of spurs and high resolution are challenges to achieving fully-integrated high-performance ADPLL architecture.

In ADPLLs, time-to-digital converters (TDCs) have been replacing conventional phase-frequency detectors (PFDs) and charge-pumps [4]. The resolution of the TDC is very important in the performance of the ADPLL because low resolution causes in-band phase noise. TDCs require advanced CMOS technology and additional system complexity to achieve high resolution and thereby have high power consumption. Additionally, TDCs are sensitive to process, voltage, and temperature variation. Such high sensitivity can cause poor linearity and non-uniform phase detector gain, resulting in widespread spur generation. Hence, we consider a TDC-less controller-based ADPLL for high performance and low complexity. The digital implementation of a controller reduces the silicon die area and eliminates external loop filter components.

This paper describes the proposed controller-based ADPLL, which is fabricated using a 130-nm CMOS process. The circuit is intended for medical implantable transceivers operating in the MICS band and is based on a programmable integer-*N* PLL. In our previous studies [5], [6], we confirmed the system stability and functionality of controller-based ADPLL through phase-domain modeling. In this paper, we focus on circuit design and implementa-

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tion details as well as measurement results in the MICS frequency band for medical applications. Section 2 presents the controller-based ADPLL architecture. Section 3 describes the circuit design and implementation. The measurement results are presented in Sect. 4, and the performance of the proposed ADPLL is compared with that of related devices previously reported in the literature. Finally, conclusions are drawn in Sect. 5.

2. Architecture of All-Digital Phase-Locked Loop

Figure 1 shows the top-level architecture of the designed ADPLL. It consists of a PFD, a controller, a digitally-controlled oscillator (DCO), a phase interpolator (PI), a phase selector (PS), and a programmable frequency divider. The proposed ADPLL has a secondary phase selection path to select the phase with the least error from the phases generated by the PI. Furthermore, the phase of the ADPLL output signal is pre-settled by the phase selection, thereby reducing the phase acquisition time of the ADPLL. The feedback path includes a programmable frequency divider that divides the output signal for comparison with a reference signal. The PFD detects both the phase and frequency differences between the reference and feedback signals (REFclk and FBclk, respectively, in Fig. 1). The pulse widths of the PFD outputs (UP and DN) indicate the phase difference. The controller then measures the UP and DN pulses to digitize the phase differences. The accumulator in the controller counts the phase error using the time resolution of the CLK of the controller. Based on the phase and frequency errors, the controller adjusts the digital control words. The frequency and phase control words are generated by the division (/) and modulo (%) operations, respectively. The DCO generates a signal whose output frequency is tuned with the digital control word $\mathrm{CNT_{freq}}$ from the controller. Based on the phase control word $\mathrm{CNT_{phase}}$, the PS selects one of the multi-phase signal generated by the PI with the least phase error. The phase of the output signal is pre-settled by phase selection, as described above.

2.1 Phase-Domain ADPLL Model

The controller-based ADPLL is a discrete-time sampled system implemented with all digital components. Therefore, the z-domain representation is the most accurate without requiring approximations [7]. Figure 2 shows the discrete-time z-domain model of the ADPLL, where K_{dco} is the gain of the DCO and K_{pi} is the gain factor from the PS. The variables $\Delta\theta_r$ and $\Delta\theta_0$ are the excess reference and feedback phases, respectively, and the sampling rate is the reference frequency f_r.

The controller has two types of digital control words based on the counter operation, and its two transfer functions $K_{cnt,dco}$ and $K_{cnt,ps}$ for the DCO and PS in discrete-time z-domain are respectively given by [5], [6]

$$K_{cnt,dco}(z)\theta_e(z) = 2^{-b_{frac}}\left\lfloor \frac{1}{M_{PI}}\frac{1}{z-1}\left\lfloor \frac{N\cdot\theta_e(z)}{2\pi}\right\rfloor\right\rfloor, \quad (1)$$

$$K_{cnt,ps}(z)\theta_e(z) = \frac{1}{M_{PI}}\frac{1}{z-1}\left\lfloor \frac{N\cdot\theta_e(z)}{2\pi}\right\rfloor - \left\lfloor \frac{1}{M_{PI}}\frac{1}{z-1}\left\lfloor \frac{N\cdot\theta_e(z)}{2\pi}\right\rfloor\right\rfloor, \quad (2)$$

where $\lfloor x\rfloor$ is the floor function, and yields the largest integer not greater than x, θ_e is the phase error, b_{frac} is the number of digits of a fractional part of the DCO input, N is the frequency division ratio, M_{PI} is the number of phases generated through the PI, and z=exp(s/f_r). The expressions on the right-hand sides of Eqs. (1) and (2) correspond to the Verilog-hardware description language (HDL) description of the controller in this study. Within a small-signal analysis, to simplify the ADPLL analysis, $K_{cnt,dco}(z)$ and $K_{cnt,ps}(z)$ are approximated as α_f+$\rho/(z-1)$ and α_p, respectively. The multiplication factors α_f and ρ are the loop parameters, and α_p is the phase compensation factor. To simplify the mathematical expressions, the scaled factors are given as α_{fn}=$K_{dco}\alpha_f/N$, ρ_n=$K_{dco}\rho/N$, and α_{pn}=$K_{pi}\alpha_p/N$.

The ADPLL has been mathematically analyzed as z-domain and linearly approximated s-domain models in [5], [6], [8]. It is common to approximate the z-transform as a linear continuous-time system in the s-domain. The sampling rate f_r must be at least 10 times the PLL bandwidth [9], such that the approximation z=exp(s/f_r)≈1+s/f_r is vaild. From Appendix, the phase selection path generates additional zero, and it affects the system parameters. As a result, the phase selection can enhance the tunability of zero in the open-loop transfer function. Generally, the closed-loop function of the ADPLL exhibits classical two-pole system behavior. For this phase model to be compared with the classical two-pole system transfer function, the phase error transfer function is expressed as

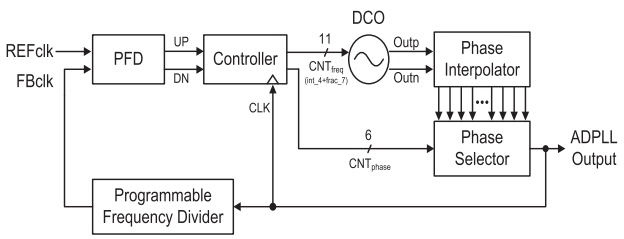

Fig. 1 Architecture of the controller-based ADPLL.

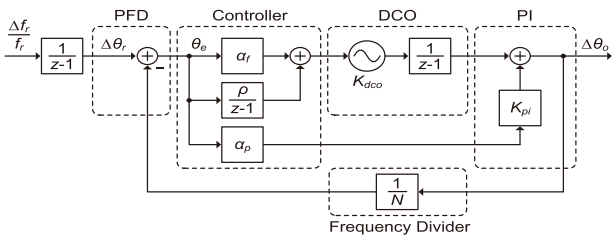

Fig. 2 z-domain model of the controller-based ADPLL.

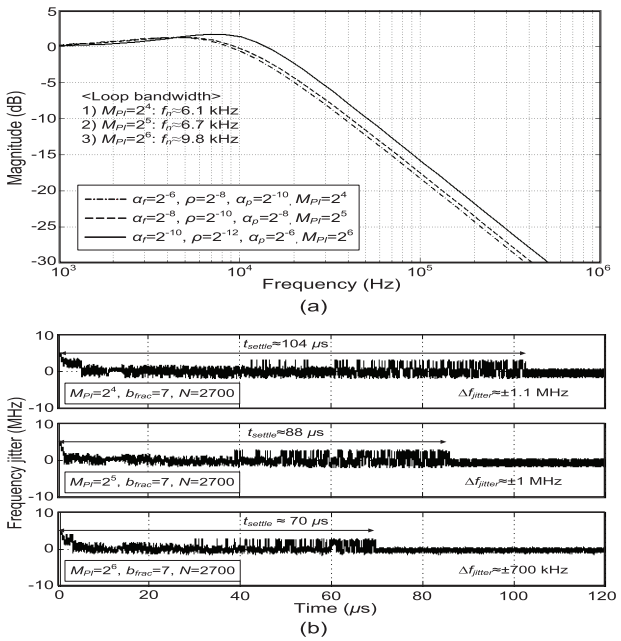

Fig. 3 (a) Magnitude response $H_{cl}(s)/N$ and (b) frequency jitter response for one-integer frequency step in the behavior-level simulation.

$$H_e(s) = 1 - \frac{H_{cl}(s)}{N} = \frac{1}{1+\alpha_{pn}} \cdot \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \quad (3)$$

where $f_n=\omega_n/2\pi=\sqrt{\rho_n/(1+\alpha_{pn})}f_r/2\pi$ is the natural frequency and $\zeta=\alpha_{fn}/2\sqrt{(1+\alpha_{pn})\cdot\rho_n}$ is the damping factor. The additional phase compensation factor α_{pn} affects factors ζ and f_n. The phase and frequency errors are eliminated by the closed-loop system. The inclusion of the phase compensation factor reduces the residual phase error of the system.

Figure 3 shows the simulation results of the phase-domain model for the s-domain approximation and the behavior model based on Verilog-HDL. The modeling parameters α_f, ρ, and α_p can be approximately expressed using M_{PI}, b_{frac}, and N. In this simulation, the gains K_{dco} and K_{pi} are 2 MHz/code-change (=4π Mrps/code-change) and $2\pi/M_{PI}$ rad/code-change, respectively. From Fig. 3 (a), as M_{PI} increases, the phase domain model simulation of the ADPLL shows that the loop bandwidth increases. The s-domain model has been validated against Verilog-HDL simulations in the previous studies [5], [6]. From the behavior-level simulation shown in Fig. 3 (b), as M_{PI} increases, the settling time and frequency jitter variation both decrease. In this study, with f_r=150 kHz, N=2700, b_{frac}=7, and $M_{PI}=2^6$ ($\alpha_f=2^{-10}$, $\rho=2^{-12}$, and $\alpha_p=2^{-6}$), f_n and ζ are 10 kHz and 0.85, respectively. Note that $f_n \ll f_r$. The settling time (=$4/\zeta\omega_n$) is less than 70 μs.

From similar behavior-level simulation results for N=27–2700 and $M_{PI}=2^4$, 2^5, and 2^6 and their comparison with the s-domain analytical model, the empirical approximations for α_f, ρ, and α_p were obtained in this study as

$$\alpha_f \approx 4\rho \approx \frac{1}{5} \cdot \frac{2^{-b_{frac}}}{2\pi} \cdot \frac{N^{1.25}}{M_{PI}^2}, \quad (4)$$

Table 1 Design considerations

Technology	130-nm CMOS process
Supply voltage	0.7 V
Power consumption	< 1 mW
Operating frequency	402 ~ 405 MHz (MICS band)
Tuning range	> 3 MHz
Frequency resolution	< 30 kHz
Phase noise	< −100 dBc/Hz @ 200 kHz offset
Settling time	< 100 μs

$$\alpha_p \approx \frac{1}{2} \cdot \frac{1}{2\pi} \cdot \frac{M_{PI}^2}{N^{1.25}}. \quad (5)$$

The variables α_f and ρ depend on the maximum number of digitized phase differences (N) and the phase resolution ($\propto 1/M_{PI}$). Equation (5) implies that α_p depends on the range of the modulo of M_{PI} (0, 1, $\cdots$, $M_{PI}-1$) and the time resolution of the CLK ($\propto 1/N$).

2.2 Design Considerations

Table 1 shows the design considerations of the ADPLL based on the MICS band requirements. In this ADPLL, digital circuits are implemented based on the standard-cell library. To ensure low power consumption, a supply voltage of 0.7 V, which is the minimum voltage for the stable operation of the employed digital standard-cell circuits, is applied. The phase noise requirement for the MICS band is less than −100 dBc/Hz at an offset frequency of 200 kHz. Additionally, the frequency tuning specifications for the DCO are derived from the intended application with a periodic calibration, where the MICS reference tolerance is 100 ppm [1]. Accordingly, the target frequency resolution considering the margin is set to less than 30 kHz. The settling time is set to less than 100 μs for low start-up energy. From behavior-level simulations, the phase interpolation technique with 64 phases is used considering the margin, and it yields a phase deviation of $2\pi/64$.

3. Circuit Design and Implementation

3.1 Phase Frequency Detector and Controller

Figure 4 (a) shows the combination of the PFD and the controller used to convert the phase difference between the reference and feedback signals from the frequency divider to digital data. The employed PFD consists of D-flip-flops (DFFs), a NOR gate, and a delay element. As shown in Fig. 4 (b), the DFFs are implemented by the true-single-phase-clock (TSPC) [10] for low-voltage operation. This structure has low power consumption and a large operating frequency range because of short gate delays in the critical reset path. Furthermore, the added delay element is helpful in preventing the dead-zone problem. It improves the phase adjustment and reduces the phase noise of the oscillator. The controller consists of an accumulator and registers to measure the PFD outputs and generates the control words. It uses a high CLK frequency to achieve high resolution. The

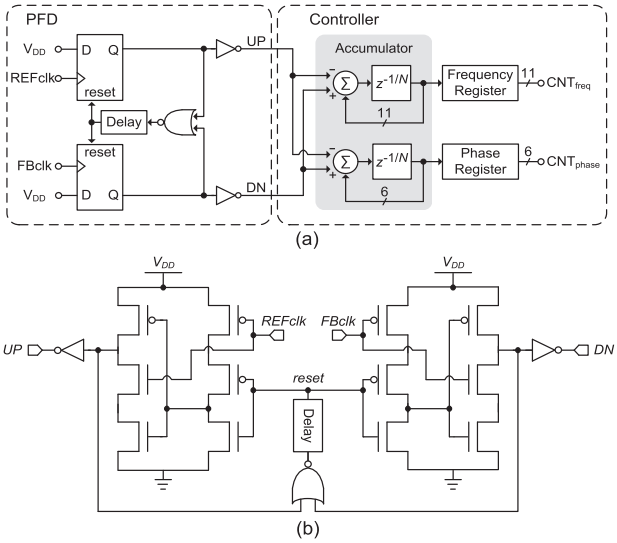

Fig. 4 (a) Structure of the PFD and controller and (b) schematic of the TSPC DFF-based PFD.

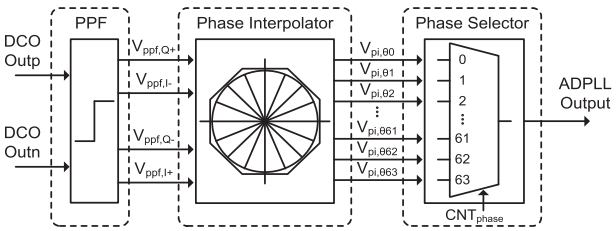

Fig. 5 Structure of the PI.

delay element in the accumulator in Fig. 4 (a) is expressed as $z^{-1/N}$. In this study, Verilog-HDL is used to design the controller. The logic-synthesizer is used to synthesize the module for gate-level circuits with a standard-cell library following a digital design flow.

3.2 Phase Interpolator

Figure 5 shows the structure of the PI. It consists of a polyphase filter (PPF), a resistive PI, and a PS. A combination of the PPF and PI is used to generate the 64-phase signal. First, quadrature signals are generated by the PPF from the DCO differential outputs. In this study, as shown in Fig. 6 (a), a two-stage RC network PPF was employed because of the wide bandwidth [11]. A two-stage PPF is useful to enhance the robustness of the process variations in passive elements [12]. Furthermore, high load impedances can reduce component mismatch. The resistor and capacitor values of the two-stage PPF are R_{p1}=100 Ω, R_{p2}=82 Ω, and C_{p1}=C_{p2}=4.42 pF. The designed PPF has a bandwidth of 350 to 450 MHz and a phase error of 0.1°. Second, an additional 15 signals are generated by the PI element, which consists of a resistor ladder between quadrature signals, as shown in Fig. 6 (b), resulting in the 64-phase signal. The resistive voltage-mode interpolator generates the interpolation outputs with a symmetric zero-crossing [13], [14]. Moreover, the resistive interpolator reduces the power consumption in comparison with a current-mode interpolator [15].

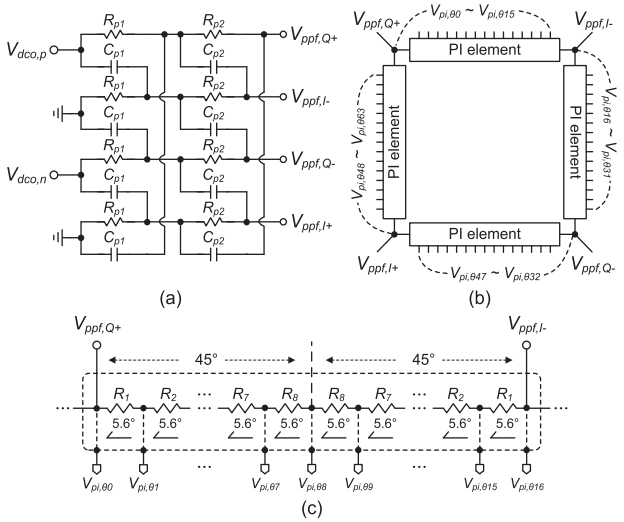

Fig. 6 Schematics of (a) the two-stage PPF, (b) the PI, and (c) a PI element (M_{PI}=2^6).

Nonlinear resistor values were used to achieve equal phase differences. Figure 6 (c) shows a schematic of the resistor ladder-based PI element. The interpolated signals are defined by the resistance ratio. The resistance ratio k_i (=$R_i/\sum_{k=1}^{M_{PI}/8} R_k$, i=1, ⋯, M_{PI}/8) of the resistor ladder can be obtained from the following equation:

$$\sum_{j=1}^{i} k_j = 1 - \tan\{(M_{PI}/8 - i)\,\phi\}, \tag{6}$$

where ϕ=45°/(M_{PI}/8) is the phase difference. In the 64-phase interpolator (M_{PI}=2^6), ϕ=5.625°. In this study, a resistance scale on the order of kΩ was used for the actual implementation of the resistor ladders. Based on the resistance ratio, the resistance of each branch resistor is R_1=1.8 kΩ, R_2=1.53 kΩ, R_3=1.34 kΩ, R_4=1.2 kΩ, R_5=1.1 kΩ, R_6=1.04 kΩ, R_7=1 kΩ, and R_8=985 Ω.

The PS selects one of them as an output signal based on the 64-phase signal according to the phase control word from the controller. This scheme ensures reliable operation and always presents 64 stabilized interpolated signals after the phase interpolation is settled. Because the output signal lock is selected among the 64 pre-settled signals generated by the PI, the output signal is always stabilized for small reference phase fluctuation.

3.3 Digitally-Controlled Oscillator

Figure 7 (a) shows the structure of the DCO, which consists of an LC-DCO core and digital logic blocks with two types of digital words (In_int and In_frac) for frequency tuning [16]. A thermometer coder employing dynamic element matching (DEM) is used to convert the input digital bit. DEM effectively eliminates component mismatches [17]. Thus, the influence of capacitor mismatch can be reduced

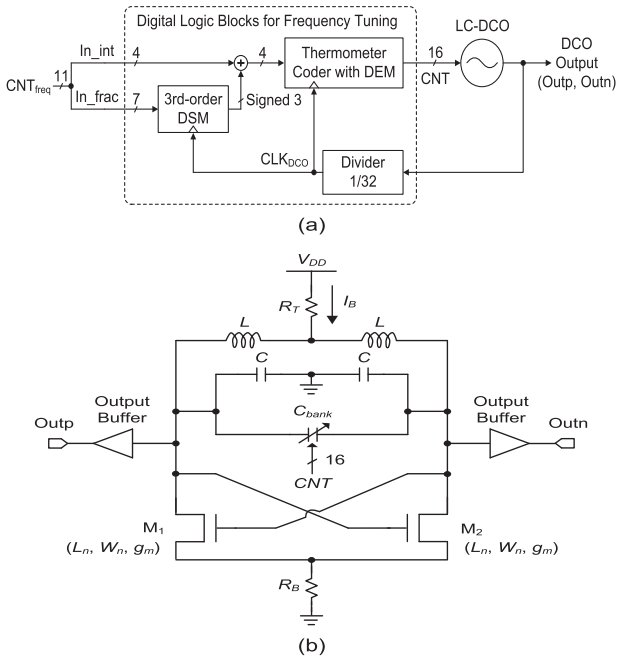

Fig. 7 (a) Structure of the DCO and (b) schematic of the LC-DCO.

by changing the capacitor selection [18]. In this study, data-weighted averaging (DWA) is considered as the DEM technique because it requires less hardware complexity and the distortion is at a higher frequency. Additionally, a third-order feedforward delta-sigma modulator (DSM) [19] is utilized to achieve precise frequency resolution. Digital tuning circuits are clocked with the high-frequency signal derived from the DCO output using a divide-by-32 circuit.

A schematic of the differential LC-DCO is shown in Fig. 7 (b). An NMOS cross-coupled pair is chosen for the oscillator core, which operates with a supply voltage of 0.7 V, because it has the advantage of common-mode noise suppression and low-voltage operation. The DCO oscillation frequency is determined by the tank inductance and capacitance. In this study, a dual-layer spiral inductor and switchable capacitor bank were used for the LC tank circuit. The inductance and Q factor of the spiral inductor L at 400 MHz were 8.18 nH and approximately 8, respectively. For low-voltage operation, a switchable capacitor bank [20] was utilized instead of a MOS varactor because it has a high Q factor, linear characteristics, and low temperature coefficients. The oscillation frequency was determined by integer and fractional frequency tuning steps. To achieve high frequency resolution (under 30 kHz), the control codes have 4-bit integer and 7-bit fractional steps. The main capacitance C corresponding to the inductance is 14.3 pF, and the tuning capacitance C_{bank} is in the range of 0.1 to 1.6 pF to span the MICS band.

The CMOS devices operating in the weak-inversion region provide high transconductance for the given bias conditions. The required NMOS device transconductance g_m that satisfies the unity loop gain at the oscillation frequency is set to 12 mS with a safety factor of 2 for stable oscillation.

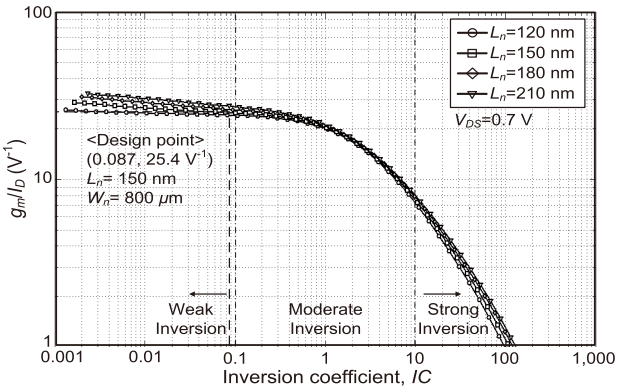

Fig. 8 Plot of g_m/I_D versus IC for difference channel lengths.

The NMOS devices were designed in the weak-inversion region to satisfy the required transconductance specification at a supply voltage of 0.7 V. The inversion coefficient IC provides a measure of the level of inversion for a given set of bias conditions and is given by [21]

$$IC = \frac{I_D}{I_0 \cdot (W_n/L_n)}, \tag{7}$$

where I_D is the drain current, I_0 is the technology current, and W_n/L_n is the device aspect ratio. Weak, moderate, and strong inversion correspond to IC<0.1, 0.1<IC<10, and IC>10, respectively. The weak-inversion operation is especially useful because g_m/I_D is nearly constant.

Figure 8 shows the simulated value of g_m/I_D plotted against the IC ratio for different channel lengths. This plot demonstrates that g_m/I_D increases with decreasing IC. In weak-inversion regions, the longer channel lengths yield higher values of g_m because longer devices have more ideal subthreshold slope factors. However, longer devices under weak-inversion would more likely result in impractically large device aspect ratios, resulting in the degradation of the unity-current-gain cut-off frequency f_T. Considering the required g_m, a channel with a length L_n of 150 nm and a width W_n of 800 μm was used for the NMOS pair transistors. Regarding this design point, g_m is approximately 12 mS, and f_T is 8.5 GHz, which is sufficient for operation in the MICS frequency band.

For the current biasing, resistive biasing with a top resistor R_T with a resistance of approximately 380 Ω is utilized because of the inherent advantage of the low noise and large voltage output swing [22]. In addition, a bottom resistor R_B with a low resistance of 10 Ω is utilized to obtain the common-mode rejection.

3.4 Programmable Frequency Divider

The employed programmable frequency divider is a pulse-swallow type system based on a dual-modulus prescaler (DMP), as shown in Fig. 9. It consists of a DMP (M/(M+1)), a pulse counter (P), and a swallow counter (S). The division ratio is determined by changing the control words of either P or S. The fundamental speed limitation of this structure

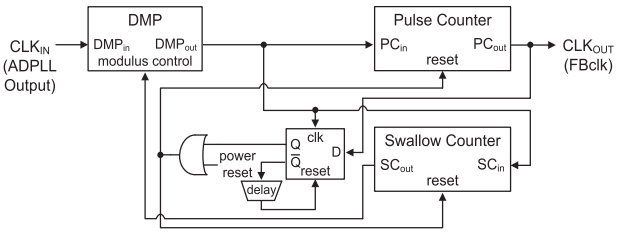

Fig. 9 Structure of the programmable frequency divider.

Table 2 Division ratios for MICS band channel selection.

Channel	CLKin (MHz)	P code (decimal)	S code (decimal)	Division ratio $D=MP+S$, $M=32$
1	402.15	83	25	2681
2	402.45	83	27	2683
3	402.75	83	29	2685
4	403.05	83	31	2687
5	403.35	83	33	2689
6	403.65	83	35	2691
7	403.95	83	37	2693
8	404.25	83	39	2695
9	404.55	83	41	2697
10	404.85	83	43	2699

usually arises from the critical delay path of the modulus control (MC) signal. This structure adopts the MC retiming scheme using a DFF [23]. The gate count and critical delay path of the MC signal extending the timing margin are reduced, which provides a low-power and high-frequency operating range in low-voltage operation. Moreover, unlike conventional complex reset circuitry with a set-reset latch and FF, the MC signal is set and reset by a single triggering signal to eliminate the unwanted offset of the total division ratio. As a result, the division ratio of the first half of each period is given by $S(M+1)$, and the second half of each period has a division ratio of $(P-S)M$. Thus, the total division ratio is simply $MP+S$. The reset circuitry is designed by tapping the divider output $\mathrm{CLK_{out}}$ and feeding it as an input to the DFF clocked with $\mathrm{DMP_{out}}$. An OR gate is used to turn off the entire divider as an external power reset. Usually, the P code is fixed, and the S code is varied to allow the selection of successive channel values. In this study, M, P, and S are set to 32, 83, 25–43, respectively, to select the 10 channels of the MICS band. Therefore, the total division ratio is 2681–2699 for the reference CLK of 150 kHz. Table 2 summarizes the required division ratios for MICS band channel selection.

4. Experimental Results and Comparison

Figure 10 shows a die photograph of the ADPLL fabricated in a 130-nm CMOS process with a supply voltage of 0.7 V. The total chip area including pads is 1.96 $\mathrm{mm^2}$, and the active chip area is approximately 0.64 $\mathrm{mm^2}$. The total power consumption of the fabricated ADPLL is 840 μW, where the DCO including the frequency-tuning and other digital blocks consume 700 and 140 μW, respectively.

Figure 11 shows the measured DCO frequency tuning

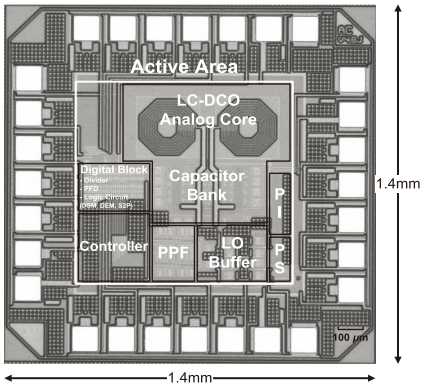

Fig. 10 Die photograph (active area of 0.8 mm × 0.8 mm).

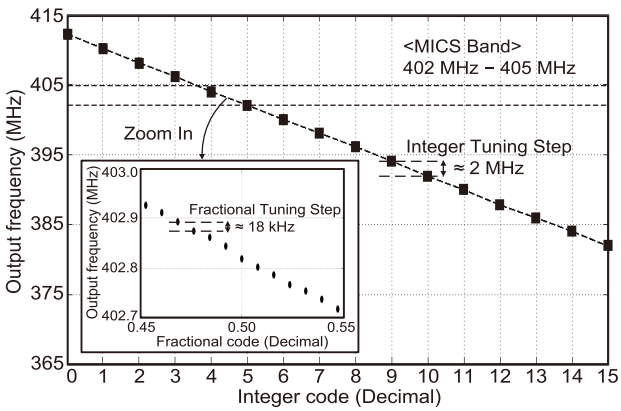

Fig. 11 Measured frequency tuning range of the DCO.

range. The fabricated LC-DCO has a wide integer frequency tuning range of 382 to 412 MHz that covers the MICS frequency band. The frequency resolution of integer tuning by 4-bit is approximately 2 MHz. The fractional frequency tuning range is achieved by using DSM. To obtain the precise fractional tuning range, data measured with the same codes are averaged. The fractional frequency resolution is approximately 18 kHz, which satisfies the target of the MICS band frequency tolerance.

Figure 12 shows the output spectrum of the ADPLL. The measured reference spur is approximately −52 dBc at an offset frequency of 150 kHz from the carrier frequency; this obtained value is similar to those obtained in related studies. As many medical applications typically operate in isolated and protected environments with relatively short communication distances, the requirement for the reference spurs is less stringent than other requirements. Figure 13 shows the measured phase noise of the ADPLL at an operating frequency of 405 MHz. Digital blocks for frequency tuning introduce a spurious tone based on the quantization noise. A DWA spur with a −120 dBc/Hz is generated at an offset frequency of 6.8 MHz. Furthermore, the DSM generates a spur at a large offset of 12.5 MHz, which is nearly equal to the clock frequency. However, the generated spur has no influence on the phase noise because it is generated at

Table 3 Performance summary and comparison

	This work	[25]	[26]	[27]	[28]
Technology	130-nm	65-nm	130-nm	130-nm	180-nm
Supply voltage	0.7 V	1.0 V	1.2 V	0.5 V	1.8 V
PLL Type	Integer-N	Integer-N	Integer-N	Integer-N	Fractional-N
VCO Type	LC-DCO	LC-VCO	LC-VCO	Ring oscillator	Ring oscillator
Operating frequency	382 MHz~412 MHz	400 MHz~405 MHz	640 MHz~650 MHz	400 MHz~433 MHz	400 MHz~410 MHz
Phase noise	−114 dBc/Hz @ 200 kHz offset	−102 dBc/Hz @ 200 kHz offset	−99 dBc/Hz @ 100 kHz offset	−92 dBc/Hz @ 1 MHz offset	−84 dBc/Hz @ 300 kHz offset
Settling time	80 μs	350 μs	500 μs	90 μs	110 μs
Reference spur	−52 dBc	−45 dBc	−52 dBc	−38 dBc	−55 dBc
Area	0.64 mm^2	0.54 mm^2	1.0 mm^2	0.072 mm^2	0.135 mm^2
Power dissipation	840 μW	430 μW	1.2 mW	440 μW	1.26 mW
FoM	−181.4 dBc/Hz	−171.8 dBc/Hz	−174.4 dBc/Hz	−147.5 dBc/Hz	−145.2 dBc/Hz

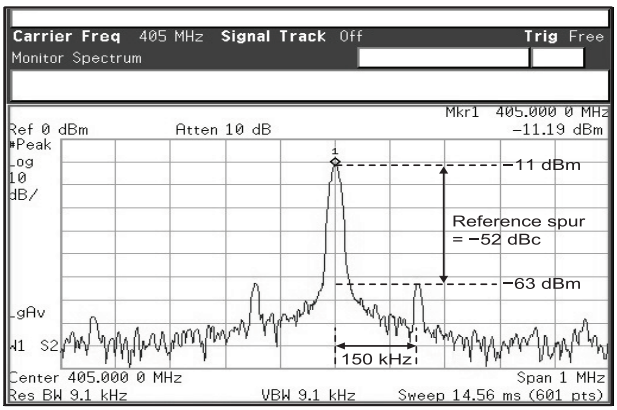

Fig. 12 Measured output spectrum of the ADPLL.

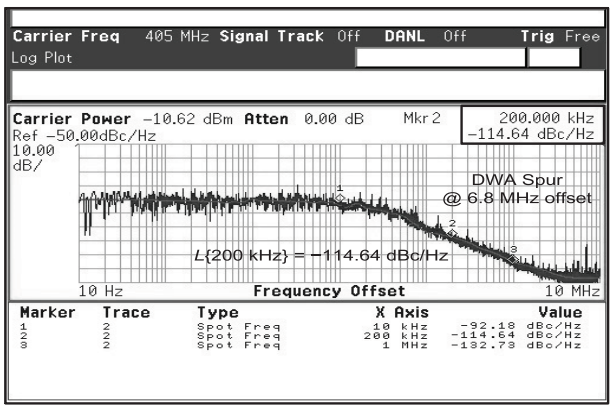

Fig. 13 Measured phase noise of the ADPLL.

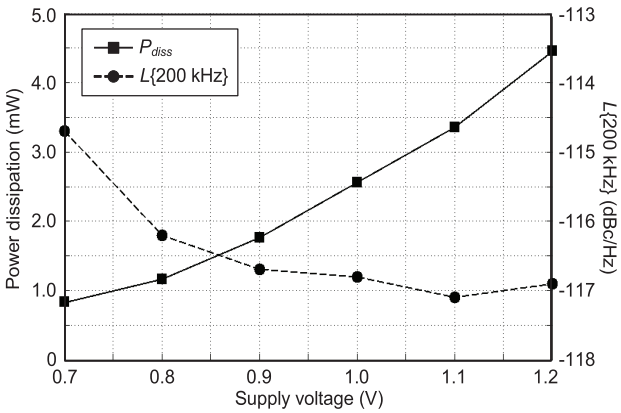

Fig. 14 Measured power dissipation and phase noise for supply voltages.

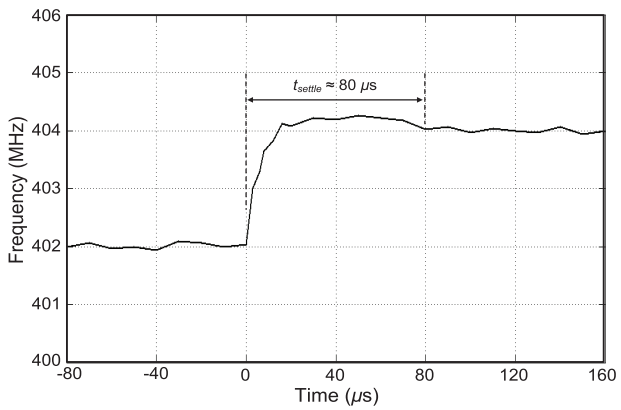

Fig. 15 Measured settling time of the ADPLL.

a large offset frequency outside of the MICS channel bandwidth. The measured phase noise at an offset frequency of 200 kHz is −114 dBc/Hz, and it satisfies the MICS band requirement. The phase noise is suppressed at a loop bandwidth of less than approximately 15 kHz and has an in-band noise of −90 dBc/Hz. Figure 14 shows the measured power consumption and phase noise for different supply voltages. The fabricated ADPLL has a wide supply voltage operating range (0.7–1.2 V).

Figure 15 shows the settling time response of the ADPLL from one locked state to another, which was taken from the integer tuning of the DCO. The settling time is approximately 80 μs with ±1% accuracy.

To evaluate the ADPLL designed in this study, the well-known figure-of-merit (FoM) is employed [24]:

$$\text{FoM} = L\{\Delta f\} - 20\log_{10}\left(\frac{f_c}{\Delta f}\right) + 10\log_{10}\left(\frac{P_{diss}}{1\text{ mW}}\right), \quad (8)$$

where $L\{\Delta f\}$ is the phase noise at an offset frequency of Δf, f_c is the oscillation frequency, and P_{diss} is the power dissipation. Table 3 summarizes the performance of the proposed ADPLL and compares this device with other PLLs

in the MICS frequency band that have been reported in the existing literature. In comparison with the devices in such related works, the proposed ADPLL demonstrates better phase noise performance and faster settling time. Low phase noise is realized by weak-inversion operation and a resistive biasing technique. The wide frequency tuning range is achieved through the switchable capacitor bank controlled by digital logic blocks. The DSM is adopted to achieve precise frequency resolution with a small number of capacitors. Additionally, the ADPLL is rapidly settled through phase selection with the PI.

5. Conclusion

A low-voltage ADPLL design for use in biomedical RF transceivers was presented in this paper. In the proposed ADPLL, controller-based loop topology is used to control the phase and frequency to yield a stable ADPLL output signal. A DSM-based DCO is employed to achieve high frequency resolution, and low phase noise is achieved through weak-inversion operation and a resistive biasing technique. Moreover, the phase error is decreased by the PS with a 64-phase signal from the PI. The ADPLL fabricated in a 130-nm CMOS process achieves good phase noise performance, a wide frequency tuning range with precise frequency resolution, and rapid settling time for MICS band applications.

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Appendix: Open Loop Analysis

The open-loop transfer function of controller-based ADPLL is expressed as

$$H_{ol}(s) = \frac{\alpha_{pn}}{s^2}\left[s^2 + 2\left(1+\frac{1}{\alpha_{pn}}\right)\zeta\omega_n s + \left(1+\frac{1}{\alpha_{pn}}\right)\omega_n^2\right], \\ = \frac{\left(1+\alpha_{pn}\right)\omega_n^2}{s^2}\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right). \quad (A\cdot 1)$$

The open-loop transfer function shows two poles at origin and two zeros at ω_{z1} and ω_{z2}, which are expressed as

$$\omega_{z1} = \left(1+\frac{1}{\alpha_{pn}}\right)\zeta\omega_n\left[1-\sqrt{1-\frac{4\alpha_{pn}\rho_n}{\alpha_{fn}^2}}\right], \\ \omega_{z2} = \left(1+\frac{1}{\alpha_{pn}}\right)\zeta\omega_n\left[1+\sqrt{1-\frac{4\alpha_{pn}\rho_n}{\alpha_{fn}^2}}\right]. \quad (A\cdot 2)$$

The controller-based ADPLL has an additional zero from the phase selection path. So, the system parameters depend on the phase compensation factor α_{pn}. In this model, the system characteristics can be controlled by adjusting the phase compensation factor α_{pn}.

For the case where α_{pn}=0, the open-loop transfer function is obtained as follows:

$$H_{ol}(s) = \frac{\omega_n^2}{s^2}\left(1+\frac{2\zeta}{\omega_n}s\right) = \frac{\omega_n^2}{s^2}\left(1+\frac{s}{\omega_z}\right), \quad (A\cdot 3)$$

where ω_z=ω_n/2ζ. This open-loop expression follows the general second-order PLL system. Comparison shows that the phase compensation factor α_{pn} can enhance tunability of zero in the open-loop transfer function.

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